IE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Colin Yates Nicholas Pasch Nicholas Eib

Serial No.:

10/006,398

Filed:

November 30, 2001

For:

Alignment Process For Integrated

Circuit Structures On

Semiconductor Substrate Using Scatterometry Measurements of Latent Images in Spaced Apart Test

Fields on Substrate

Group Art Unit:

2877

Examiner:

Lauchman, Layla G.

Atty Docket:

/ 01-234

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation 1621 Barber Lane, MS D-106 Milipitas, CA 95035 408-433-7475

Date: 20 Sept 04

Respectfully submitted,

1- FIR WI

Timothy Croll

Reg. No. 36,771